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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/925,868	09/09/97	ISBARA	M INPA:035

EXAMINER	
WELLS,K	
ART UNIT	**PAPER NUMBER**
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/925,868	Applicant(s) ISBARA
	Examiner Kenneth B. Wells	Group Art Unit 2816

☒ Responsive to communication(s) filed on *1-16-01*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-17, 19, and 20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-17, 19, and 20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

1. In view of the arguments set forth in the appeal brief filed on 1/16/01, the following new grounds of rejections are set forth.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 8 and 16 are objected to because of the following informalities: in claim 8, "a" on line 2 should be deleted. In claim 16, "a fourth preselected voltage" lacks clear antecedent basis because this voltage has already been set forth in claim 15, and thus should be recited as "said fourth preselected voltage". Appropriate correction is required.

4. Claims 1-17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson.

As to claim 1, note that Nelson discloses an RC attenuator, which is essentially all that applicant is reciting in this claim. The differences are that applicant uses a continuously-on biased FET instead of the discrete resistor shown by each of the references. However, the replacement of a discrete resistor with a continuously-on biased FET is notoriously well-known in the art

(official notice is taken) and there is obvious motivation to make such a replacement, i.e., to save chip real estate, since discrete resistors take up more space than integrated FETs acting as resistance elements. The resistor recited in the claim also fails to distinguish patentably over Nelson because it is also old and well-known in the art to add such a series resistor between the gate bias voltage and the gate of the FET for the purpose of controlling the on level of the FET (and thereby controlling the resistance value of the FET), which is an old and well-known concept to those having ordinary skill in the art. The limitations that the input and output signals are binary does not define patentably over the applied prior art because, as applicant is well aware, the type of signals that are received and output by a certain device are not part of the device (i.e., they are not structural features of the invention) and thus are merely intended use limitations which cannot distinguish a claimed structure from a prior art structure which fully meets the claim under 35 USC 102 or 103. Moreover, note that the Nelson reference suggests using binary input and output signals (see Fig. 2 of that reference). The recitation of the levels of the input or output signals cannot serve to distinguish over

Nelson because these signals are not part of the invention, i.e., they are merely intended use limitations.

As to the remaining claims which recite the half-latch (i.e., the "buffer circuit" in claims 2-5, for example) including inverter 26 and pull-up FET 28, the limitations recited therein are also considered to be well-within the ordinary skill level since the use of a half-latch for reliably switching the signal at a node (or boosting/lowering the voltage) is notoriously well-known in the art as well, and thus these claims do not define over Nelson either.

Applicant should also note the references cited on the attached PTO-892 which show the equivalence of a discrete resistor and a continuously-biased FET (as disclosed by Carroll, Figs. 1 and 2; Townley, Figs. 3-6; and Ohmi et al, Fig. 9), and the references which show examples of the well-known half-latch (applicant's recited "buffer circuit"), as disclosed by Ciraula et al in Fig. 2 and Storino et al in Fig. 2.

5. In view of the above-noted new grounds of rejection, this action is non-final.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (703) 308-4809. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Kenneth B. Wells
Primary Examiner
Art Unit 2816

February 26, 2001